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KUDIRKA & JOBSE, LLP  
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BOSTON, MA 02109

EXAMINER

MANOSKEY, JOSEPH D

ART UNIT	PAPER NUMBER
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2113

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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**Office Action Summary**

Application No.

09/933,603

Applicant(s)

BERG ET AL.

Examiner

Joseph Manoskey

Art Unit

2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 August 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☒ Claim(s) 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "270" of Fig. 2. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Specification***

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

3. Claim 22 is objected to because of the following informalities: There are two claims labeled "22" on page 42 of the specification. The second claim 22 starting at line 7 of page 43 will be referred to as claim "26" for the purposes of further examination. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 17 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 17 recites the limitation "The memory controller" and "said controller processing core" in lines 1 and 2 of claim 17. There is insufficient antecedent basis for this limitation in the claim. It is believed that claim 17 should be dependent upon claim 9 and will be interpreted as such for the purposes of further examination.

7. Claim 20 recites the limitation "said rechecking information" in lines 2 and 3 of claim 20. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 1, 2, 4, 6, 7, 9-11, 16-21, 24, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Kiyonaga et al., U.S. Patent 5,371,745, hereinafter referred to as "Kiyonaga".

10. Referring to claim 1, Kiyonaga teaches an error correction apparatus, interpreted as the implementation of a memory error management method, including a buffer memory to be accessed for error checking and correction (See Fig. 3 and Col. 5, lines 10-36). The method includes determining if an error exists in the information using ECCs (See Col. 5, lines 25-26). Kiyonaga also discloses deciding if error correction is impossible, this is interpreted as deciding if it is correctable or not correctable (See Col. 5, lines 19-20). Also, the method includes using ECCS to correct the error, which is interpreted as engaging in an error correction process (See Col. 5, lines 25-26). Finally, Kiyonaga teaches the method including retry determining to perform repeating of the accessing and error correction process, interpreted as performing a memory cell error resolution process (See Col. 5, line 64 to Col. 6, line 5).

11. Referring to claim 2, Kiyonaga discloses the information being a plurality of bits in a memory controller buffer (See Fig. 3, and Col. 5, lines 23-26).

12. Referring to claim 4, Kiyonaga teaches the use of ECCs for correcting errors contained in stored data, this is interpreted as the error correction process being a single bit error correction code that corrects single bits (See Col. 5, lines 25-26).

13. Referring to claims 6 and 7, Kiyonaga discloses the memory cell error resolution process including repeating the writing of data to the buffer (See Col. 5, line 64, to Col. 6, line 5). Kiyonaga also teaches the using retry counter for counting retries, this is interpreted as incrementing a soft-error correctable error count (See Col. 8, lines 35-45).

14. Referring to claim 9, Kiyonaga teaches a memory controller that has a communication bus and a controller for implementing a memory error management process (See Fig. 3). Kiyonaga discloses the memory controller having error correction circuitry using parity, which is interpreted as being an XOR array for providing correction to single bit errors (See Fig. 3, Col. 7, lines 39-41). Kiyonaga also teaches the memory controller having a memory buffer between the host and memory medium and coupled to the XOR array (See Fig. 3). Finally Kiyonaga teaches the system having a demodulation circuit, interpreted as the backend interface, and an interface going to a host, interpreted as a front end interface (See Fig. 3).

15. Referring to claim 10, Kiyonaga discloses the memory controller correcting errors stored data in the memory buffer, which is interpreted as detecting an error at a location in the buffer (See Col. 5, lines 23-26). Kiyonaga also teaches the controller having a retry determining circuit (See Fig. 3) for repeating the reproduction of the data and error correction, this is interpreted as the processing core directing a rewrite of the

information to said location and rechecking for an error (See Col. 5, line 64, to Col. 6, line 5).

16. Referring to claim 11, Kiyonaga teaches that the data reproduction be repeated, this is interpreted as reread of information from a physical memory medium (See Col. 5, line 64, to Col. 6, line 5).

17. Referring to claim 16, Kiyonaga discloses a retry counter for counting the number of retries, this is interpreted as the memory controller having an accumulator for storing information associated with operations of the XOR array (See Fig. 3 and Col. 8, lines 35-45).

18. Referring to claim 17, Kiyonaga teaches a retry counter in the controller that keeps count of errors and the number of times data correction was repeated, this is interpreted as the processing core keeping track of error information including counts of soft, hard, and non-correctable errors (See Fig. 3, and Col. 8, lines 35-45).

19. Referring to claim 18, Kiyonaga discloses error correction processing, interpreted as a memory error resolution process (See Col. 6, lines 24-25). Kiyonaga teaches determining if the error is impossible, this is interpreted as receiving information indicating if the error is correctable or non-correctable (See Col. 5, lines 18-20). The process repeats the data reproduction and error correction, this is interpreted as

performing a buffer refreshing process and a correctable error handling process (See Col. 5, line 64, to Col. 6, line 5). Finally Kiyonaga discloses having a limit to the number of repeating of the buffer refreshes, this is interpreted as a non-correctable error handling process (See Col. 8, lines 35-45).

20. Referring to claim 19, Kiyonaga teaches repeating the reproduction of data and error correction of the data in the buffer, which is interpreted as buffer refreshing process re-entering the corrected information into the buffer location (See Col. 5, line 64, to Col. 6, line 5).

21. Referring to claims 20 and 21, Kiyonaga teaches the using a retry counter for counting retries, this is interpreted as incrementing a soft-error correctable error count for a soft correctable error handling process (See Col. 8, lines 35-45).

22. Referring to claim 24, Kiyonaga teaches the error correction process entering into a second level and beyond, this is interpreted as performing a recursive error handling process (See Col. 6, lines 6-47).

23. Referring to claim 25, Kiyonaga teaches the error correction process determining a correction is impossible on the lowest level that determines that is incapable of being performed, this is interpreted as a predictive failure analysis (See Col. 6, lines 6-23).

***Claim Rejections - 35 USC § 103***

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

25. Claims 3, 8, 13, 14, 15, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyonaga in view of Idleman et al., U.S. Patent 6,154,850, hereinafter referred to as "Idleman".

26. Referring to claim 3, Kiyonaga teaches all the limitations (See rejection of claim 1) except for the memory controller buffer being for a disk array memory system, however Kiyonaga does teach the memory controller buffer being for a magnetic tapes for external memory of a computer system (See Col. 1, lines 16-18). Idleman discloses dual memory controllers for both a tape array and a disk array (See Fig. 3 and Col. 1, lines 11-16). It would be obvious to one of ordinary skill in the art at the time of the invention to use the memory controller that contains a buffer of Kiyonaga for the disk arrays of Idleman. This would have been obvious to one of ordinary skill in the art at the time of the invention because it memory controllers provide a method for interfacing a computer to a set of storage devices such as disks or tapes (See Col. 1, lines 4-10).

27. Referring to claim 8, Kiyonaga discloses all the limitations (See rejection of claim 1) except for the failover of the memory controller to an alternate memory controller to take responsibility of memory operations, however Kiyonaga does teach correcting errors that occur with system (See Col. 1, lines 8-10). Idleman discloses a system with dual controllers where one is the primary and the other acts as a backup (See Fig. 3 and Col. 3, lines 1-3). It would be obvious to one of ordinary skill in the art at the time of the invention to use the dual controller method of Idleman with memory controllers of Kiyonaga. This would have been obvious to one ordinary skill in the art at the time of the invention to do because if one controller should fail the other will take control without the computer getting involved (See Idleman, Col. 4, lines 42-48).

28. Referring to claims 13 and 15, Kiyonaga discloses all the limitations (See rejection of claim 9) except for the failover of the memory controller to an alternate memory controller to take responsibility of memory operations, however Kiyonaga does teach correcting errors that occur with system (See Col. 1, lines 8-10). Idleman discloses a system with dual controllers where one is the primary and the other acts as a backup (See Fig. 3 and Col. 3, lines 1-3). Idleman teaches a controller failing, this is interpreted as the input/output operation being not complete, and another controller acting as backup for the primary controller, this is interpreted as the alternate memory controller completing the input/output operation of the first controller (See Idleman, Col.3, lines 1-3 and Col. 4, lines 42-48). It would be obvious to one of ordinary skill in the art at the time of the invention to use the dual controller method of Idleman with

memory controllers of Kiyonaga. This would have been obvious to one ordinary skill in the art at the time of the invention to do because if one controller should fail the other will take control without the computer getting involved (See Idleman, Col. 4, lines 42-48).

29. Referring to claim 14, Kiyonaga and Idleman teach all the limitations (See rejection of claim 13) including a controller failing, this is interpreted as the input/output operation being not complete, and another controller acting as backup for the primary controller, this is interpreted as the alternate memory controller completing the input/output operation of the first controller (See Idleman, Col.3, lines 1-3 and Col. 4, lines 42-48).

30. Referring to claim 22, Kiyonaga discloses all the limitations (See rejection of claim 19) except for the failover of the memory controller to an alternate memory controller to take responsibility of memory operations, however Kiyonaga does teach correcting errors that occur with system (See Col. 1, lines 8-10). Idleman discloses a system with dual controllers where one is the primary and the other acts as a backup (See Fig. 3 and Col. 3, lines 1-3). Idleman teaches a controller failing, this is interpreted as a hard fault, and another controller acting as backup for the primary controller, this is interpreted as correcting a hard fault (See Idleman, Col.3, lines 1-3 and Col. 4, lines 42-48). It would be obvious to one of ordinary skill in the art at the time of the invention to use the dual controller method of Idleman with memory controllers of Kiyonaga. This

would have been obvious to one ordinary skill in the art at the time of the invention to do because if one controller should fail the other will take control with out the computer getting involved (See Idleman, Col. 4, lines 42-48).

31. Referring to claim 23, Kiyonaga discloses all the limitations (See rejection of claim 19) except for the failover of the memory controller to an alternate memory controller to take responsibility of memory operations, however Kiyonaga does teach correcting errors that occur with system (See Col. 1, lines 8-10). Idleman discloses a system with dual controllers where one is the primary and the other acts as a backup (See Fig. 3 and Col. 3, lines 1-3). Idleman teaches a controller failing, this is interpreted as the input/output operation being not complete, and another controller acting as backup for the primary controller, this is interpreted as the alternate memory controller completing the input/output operation of the first controller (See Idleman, Col.3, lines 1-3 and Col. 4, lines 42-48). It would be obvious to one of ordinary skill in the art at the time of the invention to use the dual controller method of Idleman with memory controllers of Kiyonaga. This would have been obvious to one ordinary skill in the art at the time of the invention to do because if one controller should fail the other will take control with out the computer getting involved (See Idleman, Col. 4, lines 42-48).

32. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyonaga in view of Olarig, U.S. Patent 6,038,680.

33. Referring to claim 5, Kiyonaga teaches all the limitations (See rejection of claim 5) except for using a hamming code and error syndrome to correct a bit error, however Kiyonaga does disclose using ECC to correct bits in error (See Col. 1, lines 8-13). Olarig discloses using gamming code and syndrome bits to correct a bit in error (See Col. 4, lines 25-47). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the hamming code of Olarig with the correction of bits in error of Kiyonaga. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it the hamming code indicates which bit is in error and thus allows correction of that bit (See Olarig, Col. 4, lines 45-46).

34. Claims 12 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyonaga in view of Beffa et al., U.S. Patent 6,477,662, hereinafter referred to as "Beffa".

35. Referring to claim 12, Kiyonaga discloses all the limitations (See rejection of claim 10) except for the controller fencing off a location of the error in the buffer. Beffa teaches isolating defective locations in memory, or buffer, called "partialing", this is interpreted as fencing off a location (See Col. 7, lines 18-27). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the error location in the buffer of Kiyonaga with the "partialing" of Beffa to force a rewrite to a new location in the buffer. This would have been obvious to one of ordinary skill in the art at the time of

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the invention to do because it allows a memory with defective cells to still be used (See Beffa, lines 25-27).

36. Referring to claim 26, Kiyonaga discloses all the limitations (See rejection of claim 19) except for the controller fencing off a location of the error in the buffer. Beffa teaches isolating defective locations in memory, or buffer, called "partialing", this is interpreted as fencing off a location (See Col. 7, lines 18-27). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the error location in the buffer of Kiyonaga with the "partialing" of Beffa to force a rewrite to a new location in the buffer. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows a memory with defective cells to still be used (See Beffa, lines 25-27).

### ***Conclusion***

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are examples of related error correction memory controllers.

U.S. Patent 5,463,643 to Gaskins et al.


U.S. Patent 6,151,641 to Herbert

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM  
April 23, 2004

  
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